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# Optimal Power Estimation Methodology for CXL Memory Controllers

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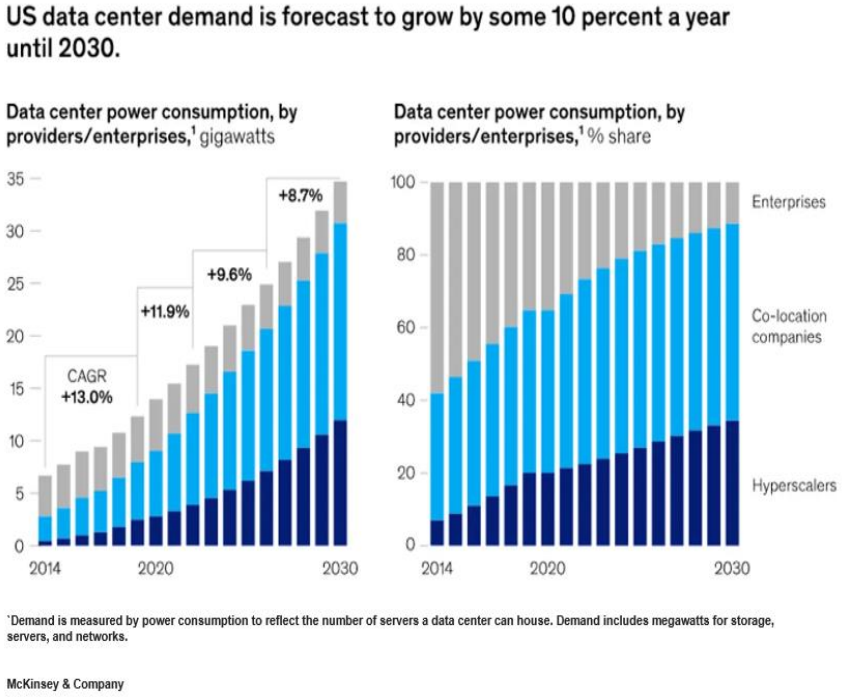
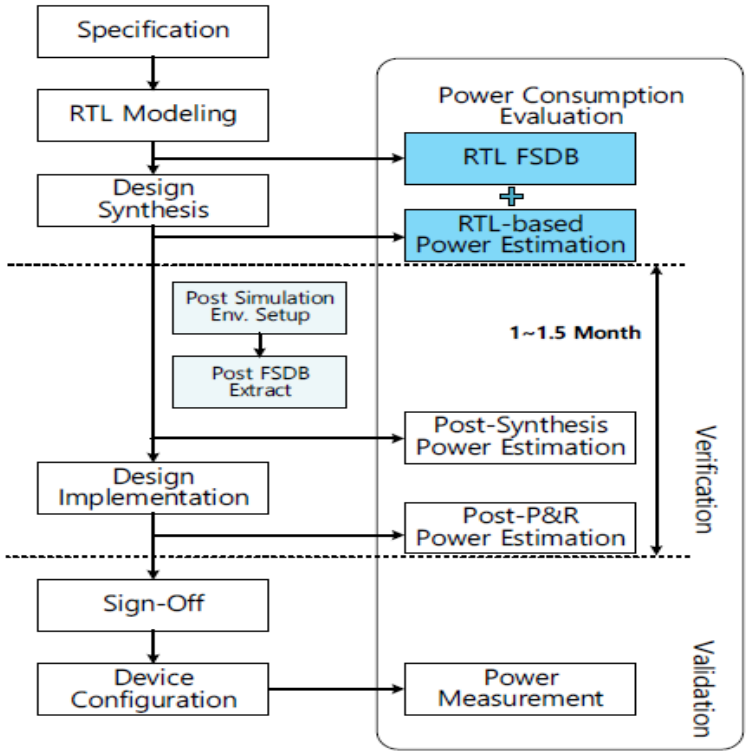
# Motivation(1/2)

- **CXL(Compute eXpress Link) Memory Controllers are Key Components for Memory Expansion and Sharing**
  - Rising AI(Artificial Intelligence) and big data workloads
  - Increasing impact of controller power consumption on overall system efficiency
  - Need finding and fixing power issues early in the design



# Motivation(2/2)

- **Challenges: Traditional Methods for Estimating Early Stage(RTL stage) Power Suffer from Inaccuracy**
  - Lack of vector generation methods
  - Need an optimal power estimation methodology
  - For accurate early stage power estimation for CXL memory controllers



# Main Idea(1/2)

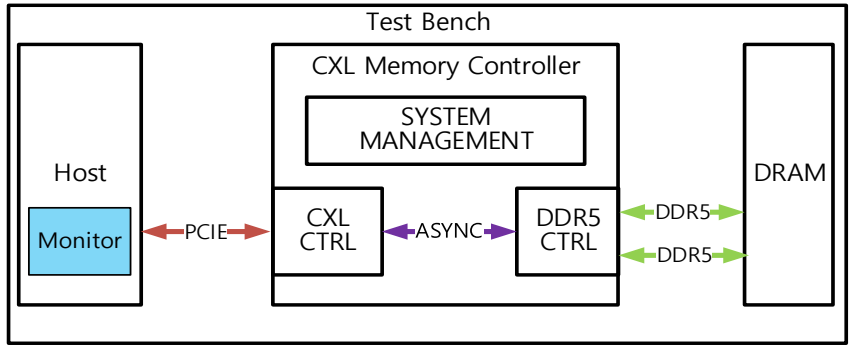
- **Proposed Methods for Generating Input Vectors**
  - Characteristic of the CXL controller for request command : Buffering
  - Leveraging the characteristics of these devices : Average Outstanding Count & Throughput

$$\bar{N}_{OC} = \frac{1}{et-st}\int_{st}^{et} N_{Outstanding\_Count}(t)dt$$

- st means start time, et means end time
- $N_{Outstanding\ Count}(t)$ means function of Outstanding Count at time t
- $\frac{1}{et-st}$ means reciprocal of the power measurement interval
- $\frac{1}{et-st}\int_{st}^{et} N_{Outstanding\ Count}(t)dt$ means an average for $N_{Outstanding\ Count}(t)$ over the power measurement interval

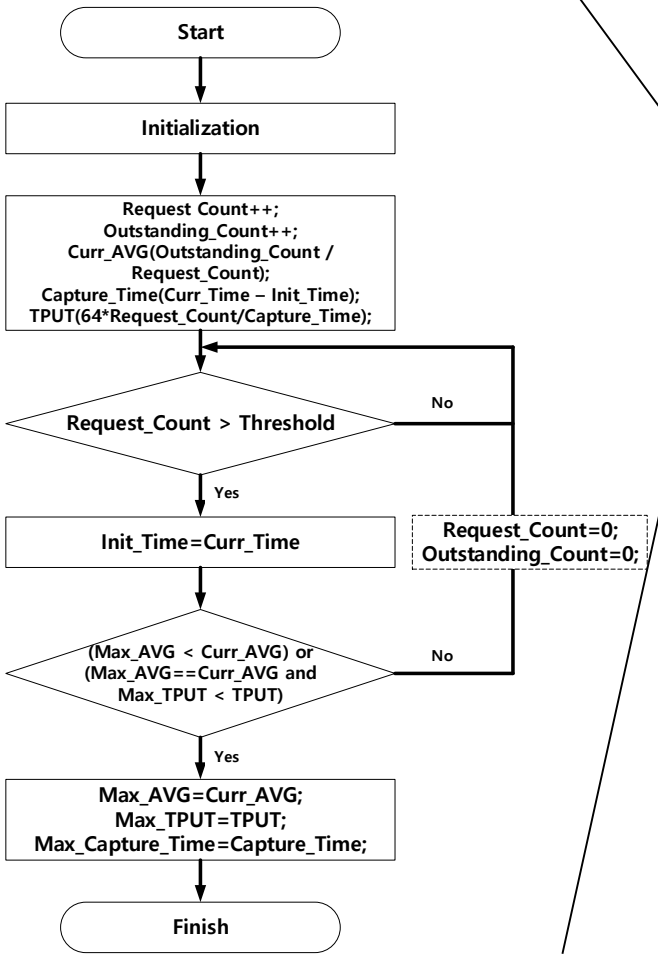
$$\overline{TPUT} = \frac{1}{et-st}\int_{st}^{et} Len_{Packet} * N_{Request\_Count}(t)dt$$

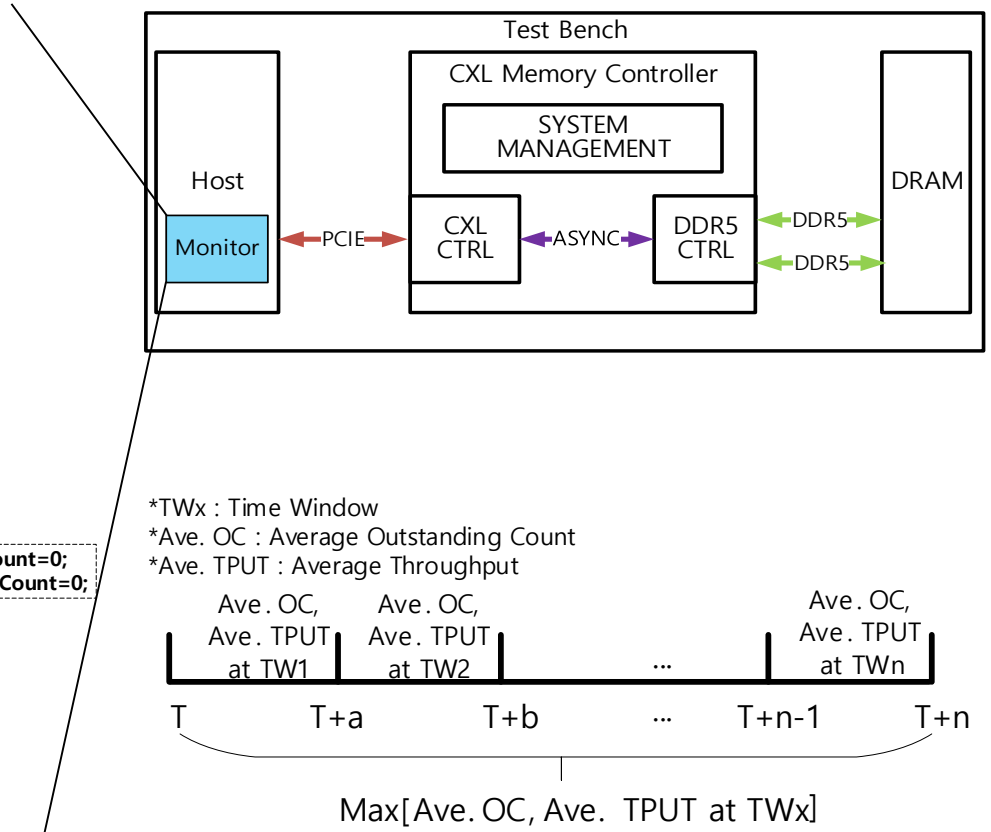
- st means start time, et means end time
- $Len_{Packet} * N_{Request\ Count}(t)$ means function of the requests number for packets with a specific length at time t
- $\frac{1}{et-st}$ means reciprocal of the power measurement interval
- $\frac{1}{et-st}\int_{st}^{et} Len_{Packet} * N_{Request\ Count}(t)$ means an average throughput for $Len_{Packet} * N_{Request\ Count}(t)$ over the power measurement interval



# Main Idea(2/2)

- **Monitor Logic To Reflect The Proposed Method**
  - Implemented packet monitoring logic
  - Measured the Average Outstanding Count, Average Throughput
  - Selecting the correct IR-Drop interval

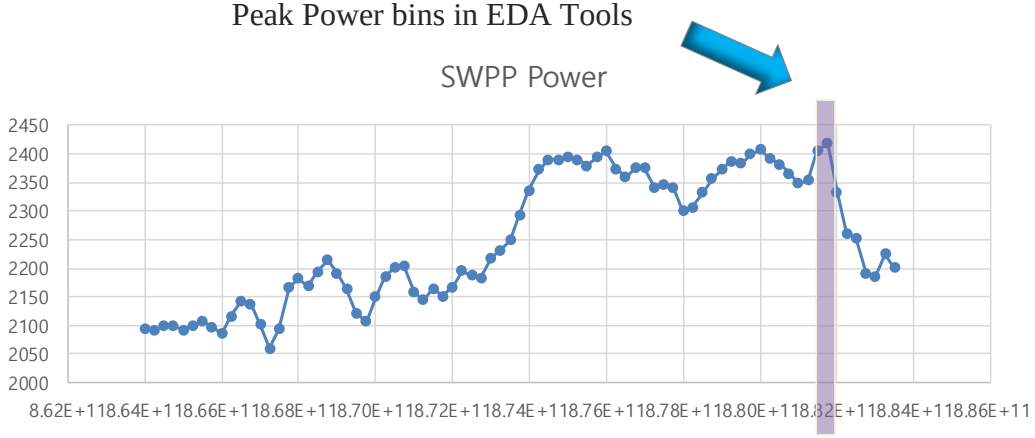


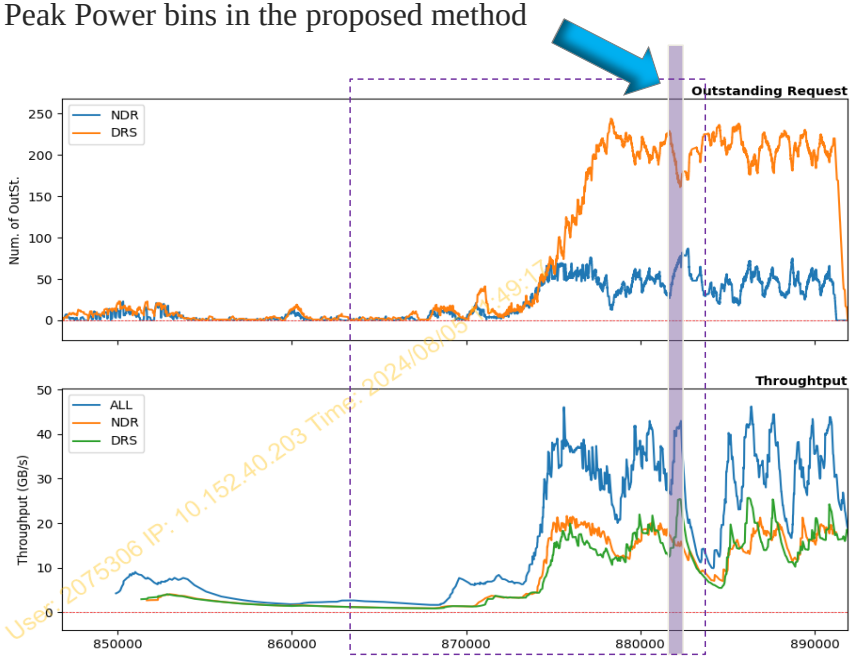
# Evidence(1/2)

- Confirmed power estimation results between gate netlist and RTL with an error rate of less than 5%
- Cross-validation with EDA tools(PowerPro) to validate proposed method

Peak Power bins in EDA Tools



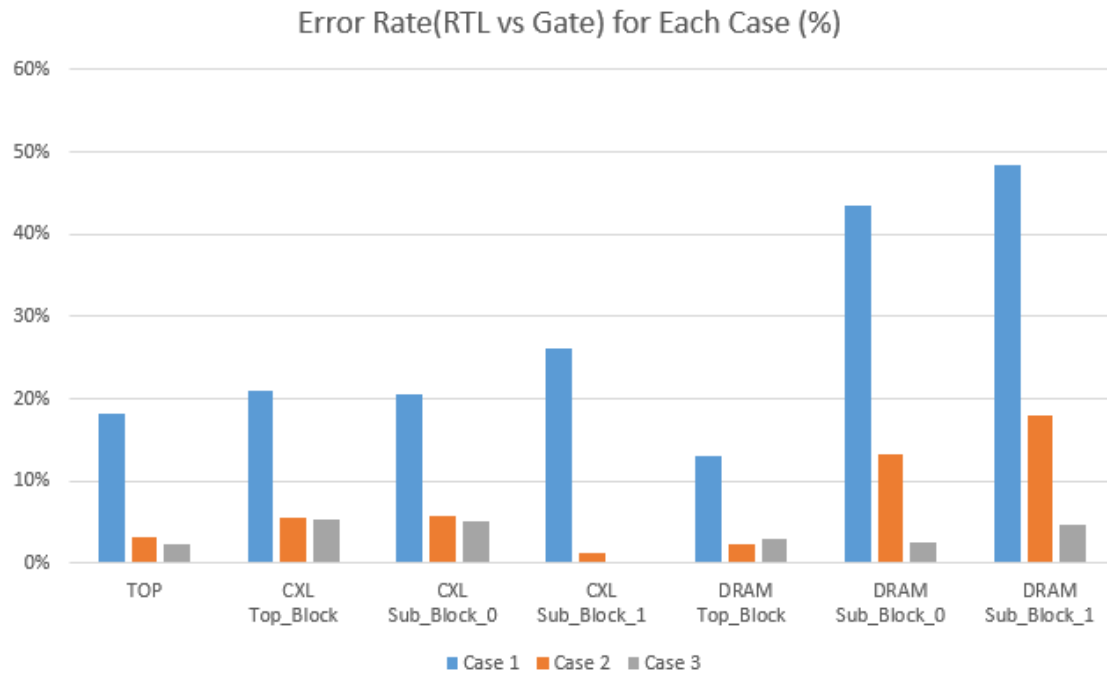

Peak Power bins in the proposed method



# Evidence(2/2)

| Block | Gate vs RTL Error Rate | Proposed Method |
|---|---|---|
| TOP | 3% | We reference the average outstanding counts and average throughput remaining in the CXL memory controller within the power measurement bin of the input vector |
| CXL_CTRL | 3% | |
| DDR5_CTRL | 5% | |

| Condition | # of Outstanding Count | |
|---|---|---|
| | Gate | RTL |
| Case 1 | 45 | 107 |
| Case 2 | 45 | 255 |
| Case 3 | 45 | 46 |



# Practical Applications

- Referencing the average outstanding counts and average throughput remaining in the CXL memory controller
- Observed that the correlation for power estimation is higher when there is less difference in the average outstanding counts between gate netlist and RTLs when the average throughput is similar
- The power estimated between gate netlist and RTL shows high correlation with less than 5% error rate
- Highly correlated RTL-based power numerical results can eliminate power-related issues in back-end design, such as power-mesh, ir-drop signoff, etc.

# Summary

- Motivation
  - Existing studies predicting power at RTL stage suffer from inaccuracies
  - Lack of vector generation methods due to different behavioral scenarios and data characteristics of different chip designs
- Methodology
  - The proposed RTL-based power estimation method for CXL Memory Controller is performed by referring the average outstanding counts and the average throughput rate within the power measurement bin of the input vector
- Main Takeaways
  - Power prediction between gate netlist and RTL shows high correlation with less than 5% error, not only to the top block of the design chip, but also to all sub-blocks
  - Cross-validate with EDA tools to validate the proposed method
  - RTL-based power numerical results estimated with high correlation are used for accurate average power and IR-drop measurements later in the design cycle
  - The method contributes to accurate and fast initial power prediction of the entire chip design and will be actively utilized in the development of the next CXL memory controller

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